What is claimed is:

1. An insulating device for system on chip (SOC), wherein the SOC has a first circuit region powered by a main power source and a second circuit region powered by a real-time power source, comprising:

a selector designating the main power source or a battery source as the real-time power source;

a level detector powered by operating power source to detect a voltage level of the main power source and output a resulting signal;

a NAND gate coupled to the first circuit and the level detector to produce a logic output according to the resulting signal and an output signal of the first circuit, wherein the NAND gate comprises:

a first NMOS transistor having a gate coupled to the output signal of the first circuit, and a source coupled to ground and a drain;

a second NMOS transistor having a gate coupled to the result signal, a source coupled to the drain of the first NMOS transistor and a drain as an output terminal;

a first PMOS transistor having a gate coupled to the gate of the first NMOS transistor, a source coupled the real-time power source and a drain coupled to the drain of the second NMOS transistor; and

a second PMOS transistor having a gate coupled to the gate of the second NMOS transistor, a source coupled to the real-time power source

and a drain coupled to the drain of the second NMOS transistor.

2. The insulating device as claimed in Claim 1, further comprising an inversion gate having an input coupled to the drain of the second NMOS transistor to invert the logic output produced by the NAND gate.

3. The insulating device as claimed in Claim 1, wherein, in normal operating mode, the main power source is designated as the real-time power source, such that the first circuit, the level detector and the power insulator are powered by the main power source.

4. The insulating device as claimed in Claim 3, wherein, in power-down mode, the battery source is designated as the real-time power, and the first circuit is not powered by the main power source.

5. The insulating device as claimed in Claim 4, wherein the resulting signal is connected to the gates of the first NMOS transistor and the first PMOS transistor without any buffer, and the output signal of the first circuit is connected to the gates of the second NMOS transistor and the second PMOS transistor without any buffer.

6. An insulating device for system on chip (SOC), wherein the SOC has a first circuit region powered by a main power source and a second circuit region powered by a real-time power source, comprising:

a selector designating the main power source or a battery source as a real-time power source;

a level detector powered by the real-time power source to detect a voltage level of the main power source and output a resulting signal;

a NOR gate coupled to the first circuit and the level detector to produce a logic output according to the resulting signal and an output signal of the first circuit, wherein the NOR gate comprises:

a first PMOS transistor having a gate coupled to the output signal of the first circuit, a source coupled to real-time power source and a drain;

a second PMOS transistor having a gate coupled to the resulting signal, a source coupled to the real-time power source and a drain as an output terminal;

a first NMOS transistor having a gate coupled to the gate of the first PMOS transistor, a source coupled to ground and a drain coupled to the drain of the second PMOS transistor; and

a second NMOS transistor having a gate coupled to the gate of the second PMOS transistor, a source coupled to the ground and a drain coupled to the drain of the second PMOS transistor.

7. The insulating device as claimed in Claim 6, further comprising an inversion gate having an input coupled to the drain of the second PMOS transistor to invert the logic output produced by the NOR gate.

8. The insulating device as claimed in Claim 6, wherein, in normal operating mode, the main power source is designated as the real-time power, such that the first circuit, the level detector and the power insulator are powered by the main power source.

9. The insulating device as claimed in Claim 6, wherein, in power-down mode, the battery source is designated as the real-time power source, and the first circuit is not powered by the main power source.

10. The a insulating device as claimed in Claim 6, wherein the resulting signal is connected to the gates of the first NMOS transistor and the first PMOS transistor without through buffer, and the output signal of the first circuit is connected to the gates of the second NMOS transistor and the second PMOS transistor without any buffer.